Q.2   a. Explain with sketches P-well process of CMOS fabrication.
Answer: Page Number 14-15 of Text Book

        b. What is the importance of Twin-Tub process? Sketch cross-sectional view
           of Twin-Tub Inverter.
Answer: Page Number 19 of Text Book

        c. Mention the advantages of CMOS over Bipolar technology.
Answer: Page Number 22 of Text Book

Q.3   a. Starting from the fundamentals derive an expression for I_{ds} of n-MOS inverter
          in saturation region and linear region**.**
Answer: Page Number 29-32 of Text Book

        b. What is Latch-up in CMOS? Sketch latch-up circuit for CMOS n-well process.
 Answer: Page Number 59 of Text Book

        c. For n-MOS enhancement transistor, μ_n = 215 cm^2/Vsec, Oxide capacitance
          (Cox) = 2.3 fF/ μm^2, drain current (I_d) = 100 μA and W/L = 10. Calculate
          Transconductance (g_m).
Answer:

W.K.T, $I_{ds} = \dfrac{\beta}{2}(V_{gs} - V_t)^2$ and $g_m = \beta(V_{gs}\text{-}V_t)$ from this we can

write Transconductance $(g_m) = (2\beta I_{ds})^{1/2} = (2.C_{ox}.\mu.\dfrac{W}{L}.I_d)^{1/2}$

$$= (2 \times 2.3 \times 10^{-15} \times 215 \times 10 \times 100 \times 10^{-6}) = 314.4 \mu mhos \;\; ohms$$

$g_m = 314.4 \mu mhos$ ohms .

Q.4   a. Discuss λ -based design rules for wires and contacts.
Answer: Page Number 74 of Text Book

        b. Draw stick-diagrams for n-MOS inverter, P-well CMOS inverter
          (i) 3-input n-MOS NOR gate
          (ii) 2-input CMOS (P-well) NOR gate
Answer: Page Number 234-235 of Text Book

Q.5   a. Show that the total delay of cascaded N number of CMOS inverters is
          $3.5\,e N\tau$.
Answer: Page Number 99-101 of Text Book

        b. Explain how Super buffers can be used to achieve symmetrical transitions,
          when inverters are used to drive more capacitive loads.
Answer: Page Number 101-102 of Text Book

c. Find the time constant (τ_p) of p-FET for the following parameters:

$(W/L)_p = 8$, $K_p = 62\ \mu A/V^2$, $V_{tp} = -0.85$ V, $V_{DD} = 3.3$ V, the total capacitance is 150 fF.

Answer:

The channel resistance of p-FET is given by

$$R_p = \frac{1}{\beta_p(V_{DD} - |V_{tp}|)}$$

$$= \frac{1}{K_p \frac{W}{L}(V_{DD} - |V_{tp}|)} \qquad = \frac{1}{62 \times 10^{-6} \times 8(3.3 - 0.85)}$$

$R_p = 822.9\ \Omega$

Now $\quad \tau_p = R_p \cdot C_p \quad = 822.9 \times 150 \times 10^{-15} \quad = 123.43\ ps$

$\tau_p = 123.43\ ps$

Q.6   a. Write the scaling factors for the following device parameters.
           (i)   Gate capacitance
           (ii) Saturation current I_{dss}
           (iii) Power speed product (P_T)

Answer: Page Number 115-118 of Text Book

         b. With truth table and stick diagram explain Bus arbitration logic for n-line bus.

Answer: Page Number 153-156 of Text Book

Q.7   a. Explain the operation of 4x4 barrel shifter with schematic. What is the limitation of 4x4 crossbar switch?

Answer: Page Number 188 of Text Book

         b. Design a single bit adder and implement 4-bit ALU functions using adder elements.

Answer: Page Number 205-206 of Text Book

Q.8   a. Explain with circuit diagram n-MOS and CMOS Pseudo-static memory cells.

Answer: Page Number 242 of Text Book

         b. Discuss briefly the ground rules for successful design.

Answer: Page Number 282-283 of Text Book

Q.9   Write short notes on:
           (i)   Design style and philosophy
           (ii) System partitioning
           (iii) Boundary Scan Test (BST)
           (iv) Built-In-Self-Test (BIST)

Answer:
     (i) Page Number 291 of Text Book
     (ii) Page Number 306 of Text Book
     (iii) Page Number 323 of Text Book
     (iv) Page Number 325 of Text Book

TEXT BOOK

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